Technology Transition in VPX

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January 2016

Technology Drivers Affecting VPX

- **Use of High Speed Internet between Modules**
  - High Speed Ethernet on Data Plane 10GBASE-KR
  - PTP IEEE 1588 within Ethernet Networks
- **Use of PCIe Gen 3 in VPX Systems for Data Plane**
- **Need for new Clock schemes**
- **High Performance Single Board Computers**
  - Native 10GBASE-KR Ethernet Ports
  - Up to 16 Core, Server on Board
- **System on Chip FPGA solutions**

Increased Chip Density Drives SWaPc

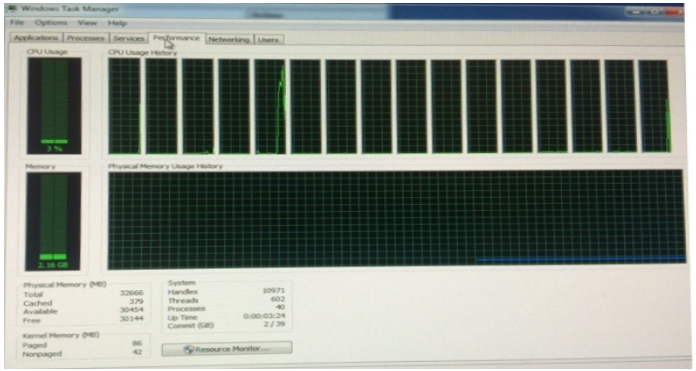
- **Increased Chip Density and System On Chip solutions allow board functionality to increase**
- **Box level solutions can be implemented at the Board level**
- **Examples Include:**
  - Servers reduced new Xeon – D multi-core Processor
  - High Speed Ethernet switches now available in 3U VPX provide necessary connectivity
  - FPGA System on Chip solution allow entire sub-systems to be placed on a 3U card

Server Class Intel SBC on 3U VPX

Boxes Becoming Board: Examples

Intel XEON – D
32 GB DDR4 Memory
8 and 16 Core CPU
Native 10Gb Ethernet

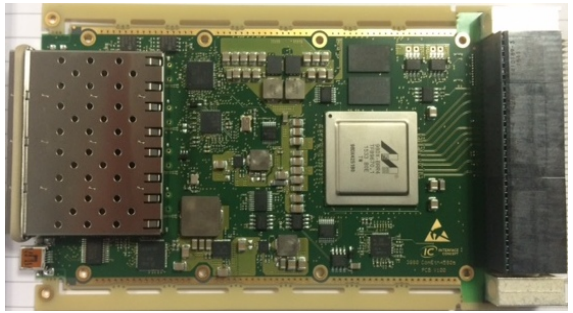
Activity Monitor
Presents 16 Threads on 8 Core Processor



High Speed 3U VPX Switch

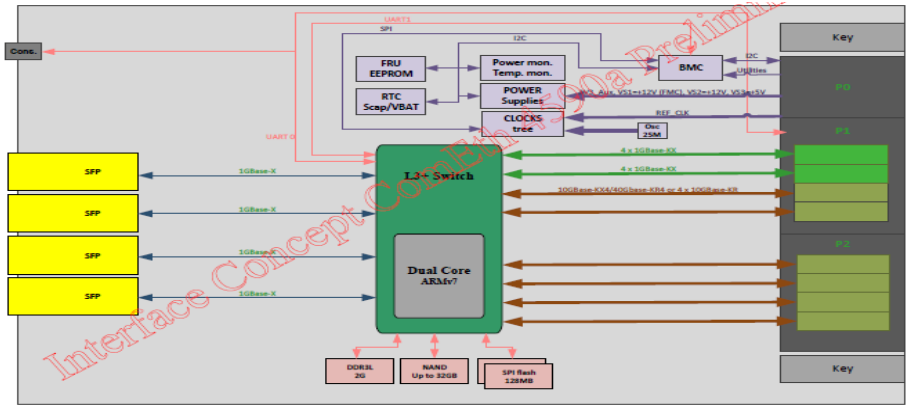
Fabric Supports

- 1000BX
- 10GBASE-KR
- 40GBASE-KR
- 10GBASE-SR



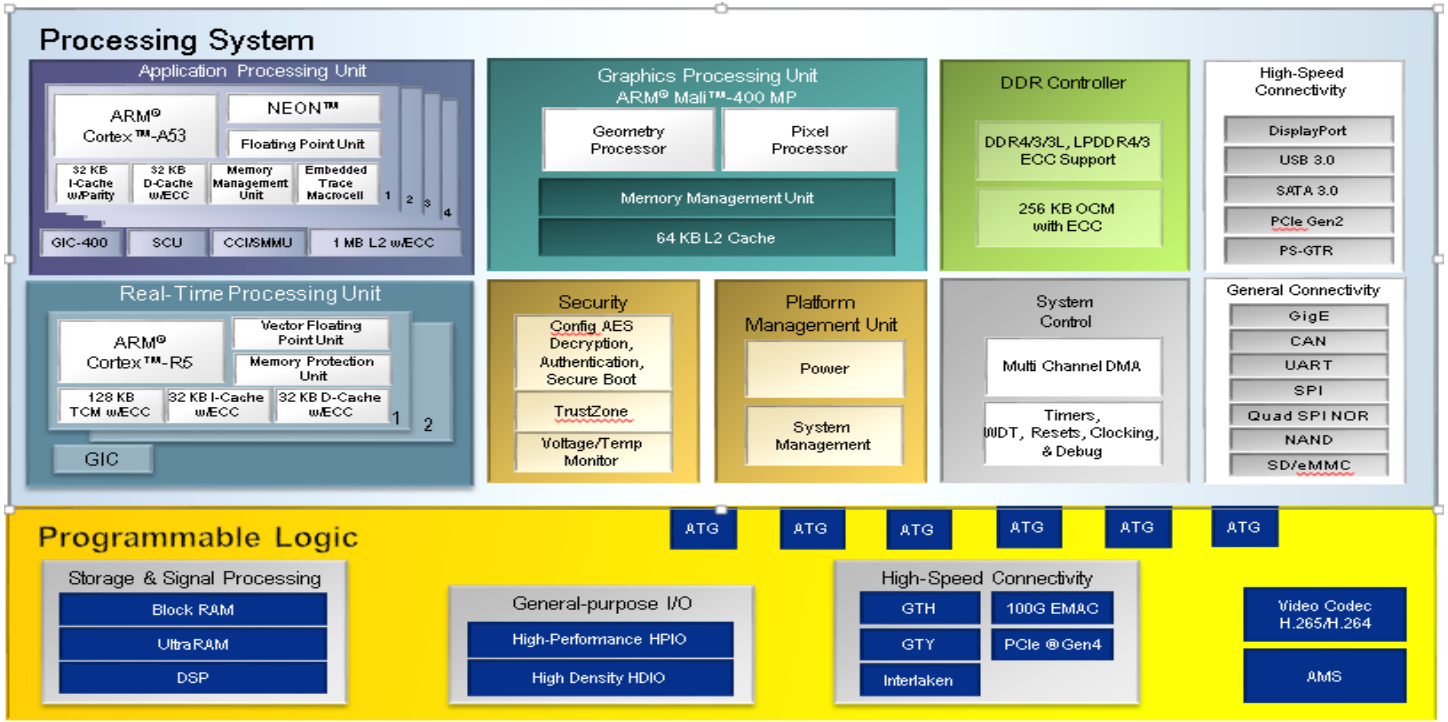
Marvel Fabric with integral ARM Processor

- 24 High Speed Ports
- 8 1000BASE-BX Ports



FPGA System On Chip

Xilinx Ultrascale Dual ARM with GPGPU



FPGA System On Chip

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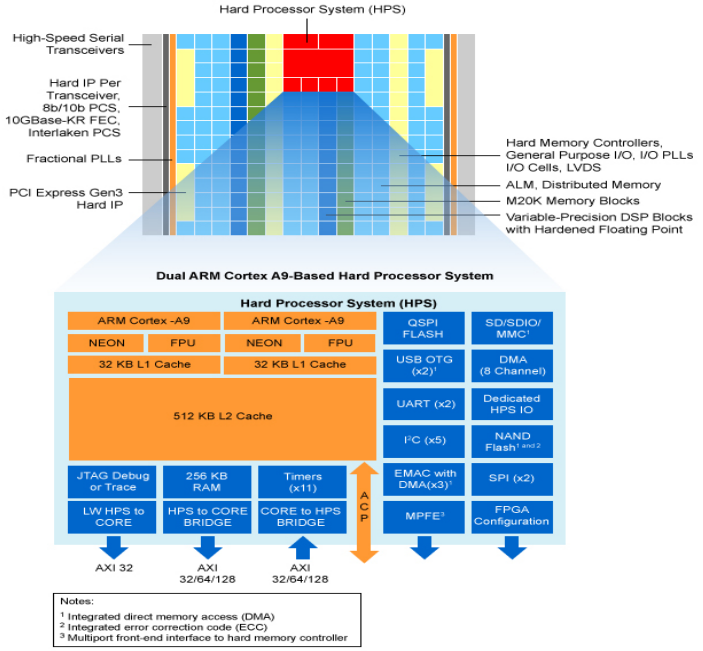
Altera Arria 10 with Integral ARM Core



FPGA System On Module Approach

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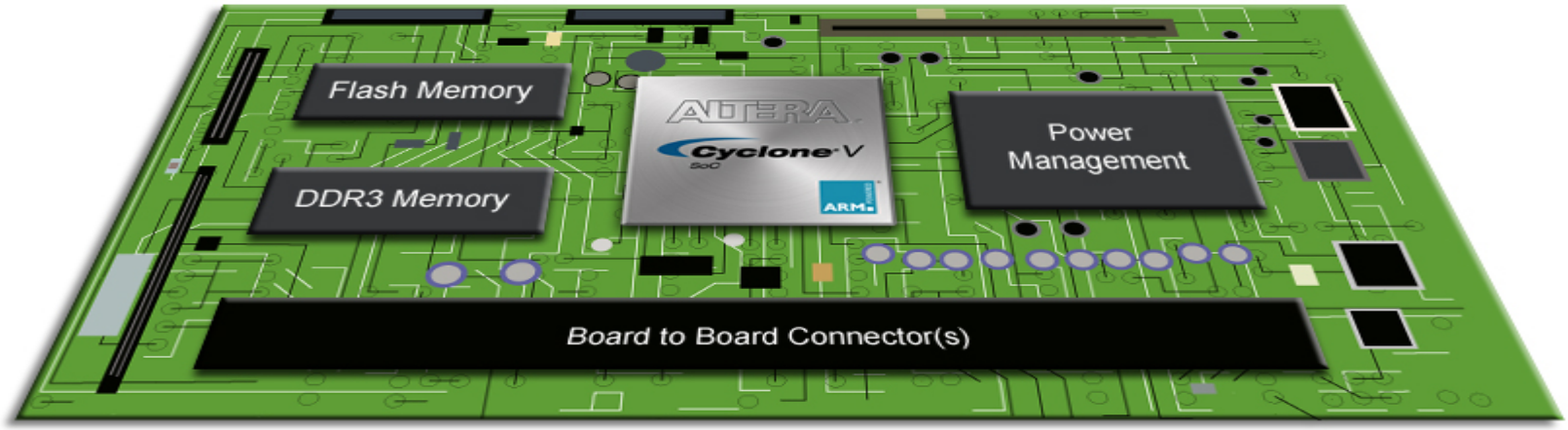
Altera System on Module: Saves design time

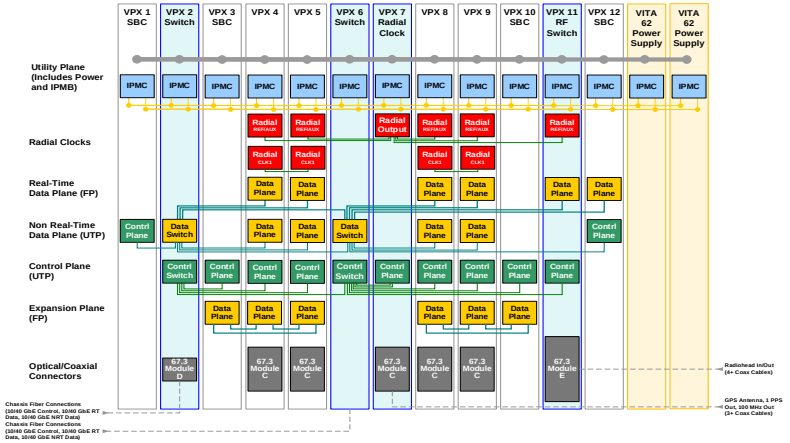


What's New in Hardware Convergence Architecture

Factors affecting VPX System Design

- **High Speed Interconnect**
  - 10.3125 10GBASE-KR
  - Date Plane use 10Gb Ethernet
- **New Connectors to Support I/O**
  - Fiber Optic
  - Coax for RF
- **Radial Clock Schemes**
  - 100 MHz Ref CLK
- **Power Density per slot**
  - 45 Watts per Module in many cases

CERDEC Converged Topology Diagram



CERDEC: Hardware Converged Architecture

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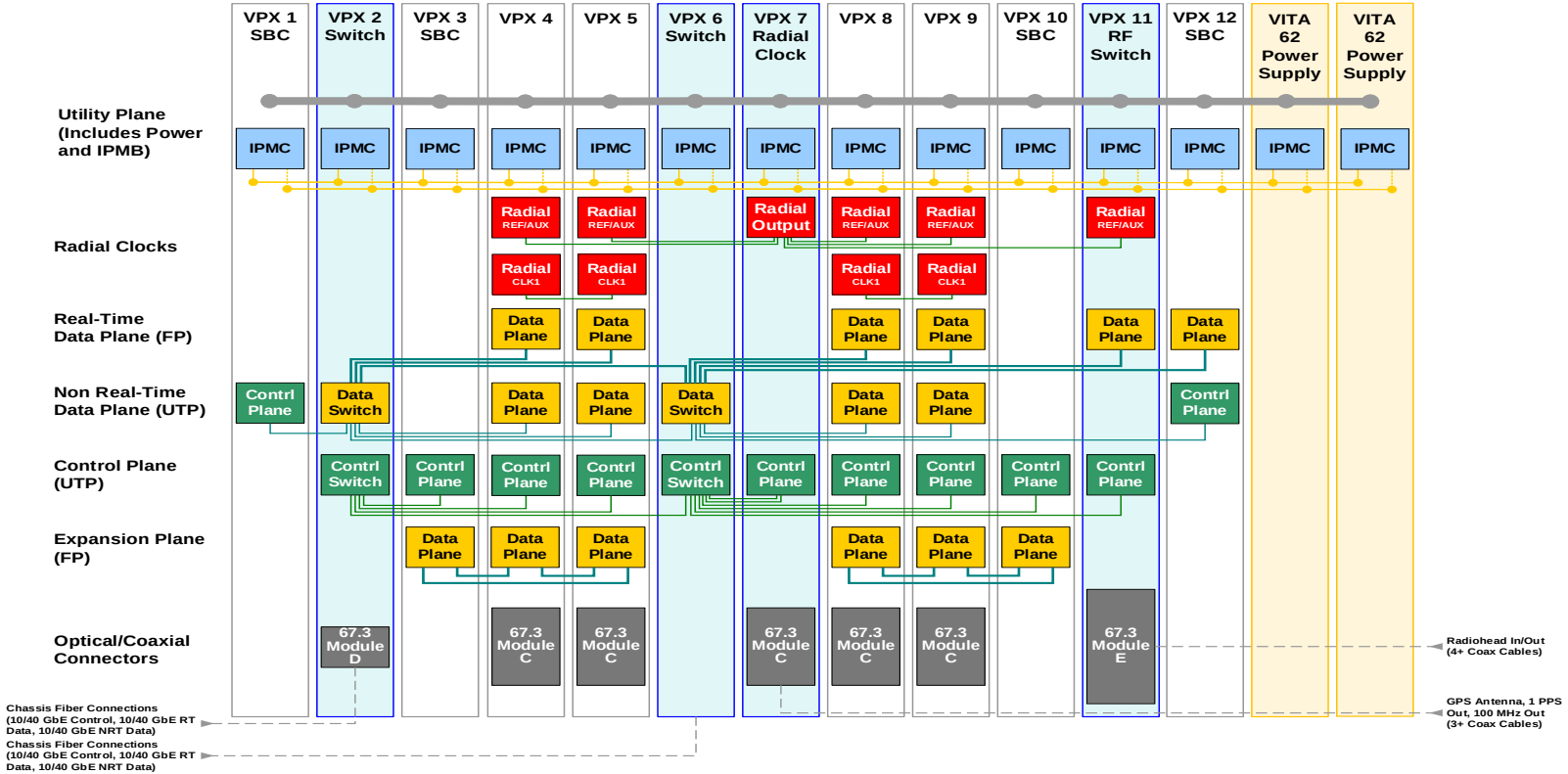


Impacts to the Backplane

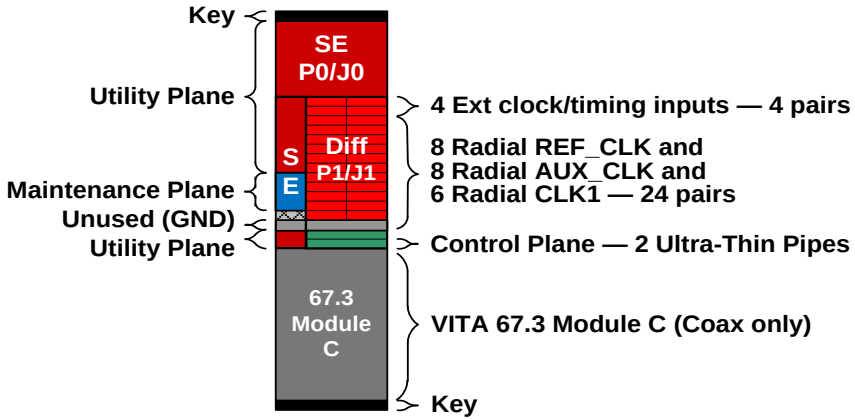
- **Backplane**
  - High speed interconnect on control and data plane
  - 10.325 Gb/sec requires extensive SI modeling
- **PCB material is changed**
  - FR4 is replaced by Megtron-6
- **Layer count increases with Signal Density**
  - Count increase from 12 to 18 layers to 24 go 32 layers
  - Max layer count is 40 layers
- **Multi-Gig connector becomes a bottle neck**
  - Isolation an in the connector is an issue
- **Good news is the backplanes can be built using the current connector and with new materials**

Specification Addressing Change

- Open VPX VITA 65
- Follow On to FMC Specification: VITA 57.1
- Cooling Specifications: VITA 48
- Channel Specification: VITA 68 defining high speed channels
- Connector Specification: VITA 67.3

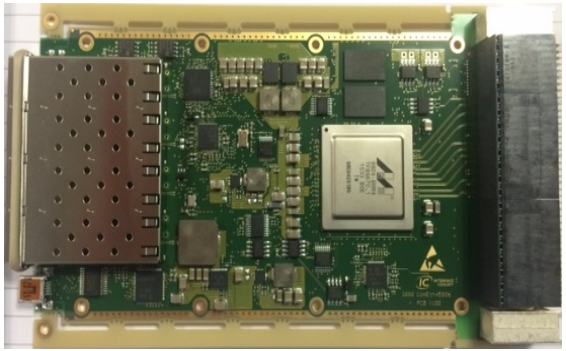
New VPX Clock Technology

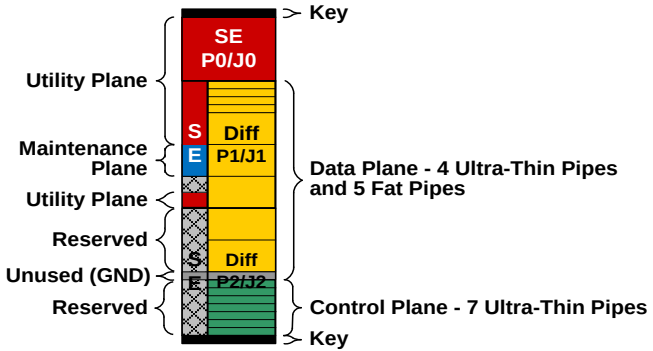
- **Radial Clocks**
  - Support skew adjusted Ref Clocks
  - New lines for high speed sampling clocks
- **Radial Clock Slot**
  - Generates and Distributes Clocks
  - Provides 1 pps Aux Clock Signal



New VPX Switch Profiles

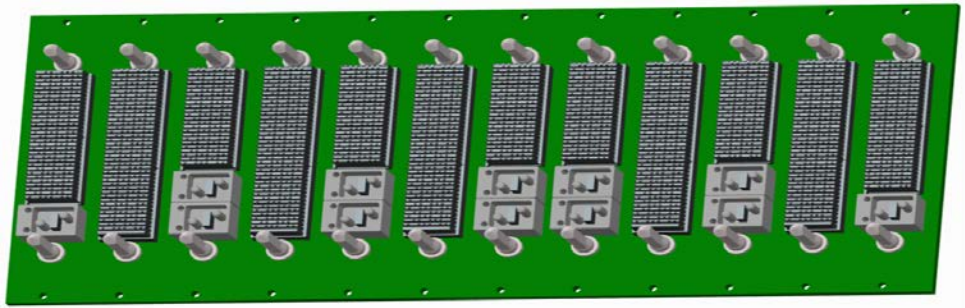
- High Speed Switch Profile Definition
- Control and Data Plane Support 10GBase-KR
- UTP support 1000BX and 10GBASE-KR
- FP support 10GBASE-KX4 and 40GBASE-KR

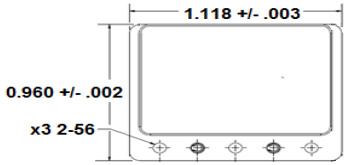




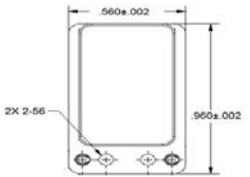
New I/O Connectors

Vita 67.1 RF and Vita 66.4 for Optical



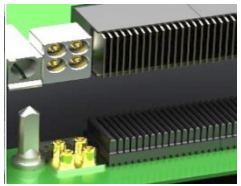


Module 67.3c

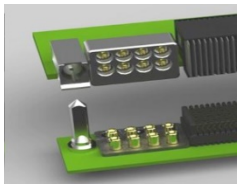


Module 67.3d

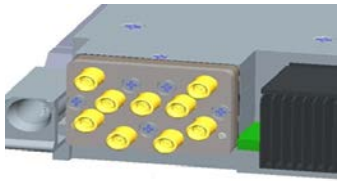
VITA 67.1 and 67.2 Module Connectors can mate with VITA 67.3 Backplane Connectors



VITA 67.1



VITA 67.2



VITA 67.3C

Module 67.3e

VPX Road Map

- **Greater Use of Fiber Optic I/O Going Forward**
  - 100Gb Ethernet requires 25Gb per lane requiring fiber optic I/O to implement off board connections
  - Next Generation Multi-Gig connector will not support this rate
- **PCIe Gen 4**
  - Doubles bandwidth from 8 GT/s per lane to 16 GT/sec per lane → BW per lane 2GB/s
- **New Multi-Gig Connector required for next generation protocols**
  - T/E connectivity indicates the design is being worked

Summary

- VPX is evolving to support new architectures
- New I/O types are being supported in VPX allowing high density fiber to be used
- RF I/O is supported for Mezzanines with VITA 67.3
- New VPX connectors will provide a path to support PCIe Gen 4
- High Speed backplanes can be built to support the bandwidth, and I/O connectors required by new architectures
- VPX systems will provide the feature set to be the platform for long life cycle systems